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EXAMINER

GRAYBILL, D

ART UNIT

PAPER NUMBER

2814

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

# Office Action Summary

Application No.  
09/029,608

Applicant(s)  
Fukusawa et al.

Examiner  
David E. Graybill

Group Art Unit  
2814



☒ Responsive to communication(s) filed on 17 Feb 2000

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

## Disposition of Claim

☒ Claim(s) 1-12 and 18-108 is/are pending in the application

Of the above, claim(s) 1-12, 20-35, 37-40, 44-53, 65-69, 71, 78, 86, 92-94, and 103-108 is/are withdrawn from consideration

☒ Claim(s) 70, 72-77, 95, and 96 is/are allowed.

☒ Claim(s) 18, 19, 36, 41-43, 54-64, 79-85, 87-91, and 97-102 is/are rejected.

☐ Claim(s) \_\_\_\_\_ is/are objected to.

☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.

## Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on \_\_\_\_\_ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some\* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) \_\_\_\_\_

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\*Certified copies not received: \_\_\_\_\_

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s) 6, 11, 12 and 15

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

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In the restriction requirement mailed 1-19-00 the indication that claims 87-91 and 95-102 are drawn to the process of Group I, and that claims 92-94 are drawn to the product of Group II is incorrect. Instead, claims 87-91 and 95-102 are drawn to the product of Group II, and claims 92-94 are drawn to the process of Group I.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 62, 79-85, 90, 97-100 and 102 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The following lack sufficient literal antecedent basis:

Claim 62 "the protruding electrodes";

Claim 79 "the wiring pattern through holes";

Claim 90 "the external connection electrodes";

The following lack sufficient literal antecedent basis to the degree that the claims are incomprehensible and cannot be further reasonably examined on the merits:

Claims 97-100 and 102 "the resin sealing step";

Claims 97, 99 and 100 "the mold";

Claims 97, 98 and 102 "the sealing resin";

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Claim 100 "the protruding electrode exposing step," and "the ends of the protruding electrodes."

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 18, 19, 36, 42, 43, 57-64, 71 and 87-91 are rejected under 35 U.S.C. 102(e) as being anticipated by Kata (5897337).

At column 4, line 7 to column 14, line 50 Kata teaches:

18. A semiconductor device comprising: a semiconductor element having a surface on which protruding electrodes 44 are formed; and a resin layer 43 which is formed on the surface of the semiconductor element and seals at least a lateral surface of the protruding electrodes.

19. The semiconductor device as claimed in claim 18, further comprising a heat radiating member 46 provided on a back surface of the semiconductor element opposite to the surface thereof on which the protruding electrodes are provided.

36. A semiconductor device comprising: a semiconductor element having a surface on which external connection electrodes 44 are provided which are to be electrically connected to external terminals; and a resin layer 43 provided on the surface of the semiconductor element so as to

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cover the external connection electrodes, wherein the external connection electrodes are exposed at a lateral surface of the resin layer.

42. A semiconductor device comprising: a semiconductor element having protruding electrodes 44 formed on a surface thereof; a first resin layer 43 that is formed on the surface of the semiconductor element and seals the protruding electrodes except for ends thereof; and a second resin layer 46 provided so as to cover at least a back surface of the semiconductor element.

43. A semiconductor device comprising: a semiconductor element having protruding electrodes 44 formed on a surface thereof; a resin layer 43 which is formed on the surface of the semiconductor element and seals the protruding electrodes except for ends thereof; and external connection protruding electrodes 44 provided to the ends of the protruding electrodes exposed from the resin layer.

57. A semiconductor device comprising: a single or a plurality of semiconductor elements; a sealing resin 46 which seals partially or totally the semiconductor element or elements; and an electrode plate 60 which is provided in the sealing resin and is electrically connected to the semiconductor element or elements, the electrode plate having portions 67 which are exposed from side surfaces of the sealing resin and function as external connection electrodes.

58. The semiconductor device as claimed in claim 57, wherein the semiconductor element or elements are connected to the electrode plate in a flip-chip bonding formation.

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59. The semiconductor device as claimed in claim 57, wherein the electrode plate is exposed from a bottom surface of the sealing resin in addition to the side surfaces thereof, so that portions of the electrode plates exposed from the bottom surface function as external connection terminals.

60. The semiconductor device as claimed in claim 57, wherein protruding terminals are provided to the electrode plate, and are exposed from a bottom surface of the sealing resin, so that the protruding terminals function as external connection terminals.

61. The semiconductor device as claimed in claim 60, wherein the protruding terminals are portions of the electrode plate 71-1 defined by plastic deformation.

62. The semiconductor device as claimed in claim 60, wherein the protruding terminals are the protruding electrodes arranged to the electrode plate.

63. The semiconductor device as claimed in claim 57, wherein the semiconductor element or elements are partially exposed from the sealing resin.

64. The semiconductor device as claimed in claim 57, further comprising a heat radiating member 64 in a position close to the semiconductor element or elements.

71. A mounting arrangement for mounting a semiconductor device on a mounting board, the semiconductor device comprising: a single or a plurality of semiconductor elements; a sealing resin 46 which seals partially or totally the semiconductor element or elements; an electrode plate 60 which is provided in the sealing resin and is electrically connected to the semiconductor element or elements, the electrode plate having portions 67 which are exposed from side surfaces of the sealing resin and function as external connection electrodes; and protruding terminals

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provided to the electrode plate, and exposed from a bottom surface of the sealing resin, so that protruding terminals function as external connection terminals: the mounting arrangement comprising: bumps 67 arranged to the protruding terminals for forming the external connection terminals, the semiconductor device being connected to the mounting board through the bumps.

87. A semiconductor wafer on which semiconductor elements are provided, comprising: a semiconductor wafer 40 including a plurality of semiconductor elements having a surface on which protruding electrodes 44 are formed; and a compressed resin layer 43 which is formed on the surface of the semiconductor elements and seals at least a lateral surface of the protruding electrodes.

88. A semiconductor device comprising: a semiconductor element having a surface on which protruding electrodes 44 are formed; and a compressed resin layer 43 which is formed on the surface on the semiconductor element and seals at least a lateral surface of the protruding electrodes, wherein a lateral surface of the resin layer and a lateral surface of the semiconductor element have planes cut by a dicer.

89. A semiconductor device as claimed in claim 88, wherein the lateral surface of the resin layer and the lateral surface of the semiconductor element have a common plane cut by a dicer.

90. A semiconductor device comprising: a semiconductor element having a surface on which connection electrodes 44 are provided, which are to be electrically connected to external terminals; and a resin layer 43 provided on the surface of the semiconductor elements so as to cover the external connection electrodes 44, wherein the external connection electrodes 44 are

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exposed at a lateral surface of the resin layer, the lateral surface of the resin layer and the lateral surface of the semiconductor element have planes cut by a dicer.

91. A semiconductor device comprising: a semiconductor element having a surface on which protruding electrodes 44 are formed; and a resin layer 43 which is formed on the surface on the semiconductor element and seals a lateral surface and a top of the protruding electrodes wherein the lateral surface of the resin layer and the lateral surface of the semiconductor element have planes cut by a dicer.

101. The semiconductor device as claimed in claim 88, further comprising a heat radiating member 46 provided on a back surface of the semiconductor element opposite to the surface thereof on which the protruding electrodes are provided.

To further clarify the teaching of the electrode plate having portions 67 which are exposed from side surfaces of the sealing resin 46, and wherein the electrode plate is exposed from a bottom surface of the sealing resin in addition to the side surfaces thereof, it is noted that Kata teaches this product at column 8, lines 50-55; and column 8, line 63 to column 9, line 1.

To further clarify the teaching of a compressed resin layer 43, it is noted that Kata teaches this product at column 8, lines 23-24 because the resin layer is inherently compressed when the film is pressed.

To further clarify the teaching of a resin layer 43 which seals a top of the protruding electrodes, it is noted that the resin layer seals a top of the lateral surface of the electrode. In any case, there is no absolute frame of reference recited; therefore, it is inherent that for any particular

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sealed portion of the electrode, an absolute frame of reference can be chosen in which the portion is a top of the electrode.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kata.

Kata is applied to the rejection as it is applied to the rejection of claim 18.

Kata does not appear to explicitly teach:

41. The semiconductor device as claimed in claim 18, wherein the resin layer comprises a plurality of resin layers having different characteristics.

Regardless, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization

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to form the resin layer of Kata wherein the layer comprises a plurality of resin layers by splitting the step of forming the resin layer into a plurality of steps of forming a plurality of resin layers. Indeed, it has been held that the splitting of one step into two, where the processes are substantially identical or equivalent in terms of function, manner and result, is prima facie obvious absent a disclosure that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical; *Ex parte Rubin* 128 USPQ 159. Furthermore, it is inherent in the resin layers so produced that the layers would have different characteristics. For example, they would each have a different characteristic of age and location.

Claims 54-56 are rejected under 35 U.S.C. 102(e) as being anticipated by Kitahara (5568363).

At column 5, line 25 to column 16, line 34 Kitahara teaches the following:

54. A semiconductor device comprising: a semiconductor element 1; protruding electrodes ("circular-arc form") functioning as external connection terminals; a wiring board 4 having a flexible base 41 on which leads 3 are formed, the leads having ends 31 connected to the semiconductor element and other ends 32 connected to the protruding electrodes; and a sealing resin 2 sealing the semiconductor element, wherein there are provided extending portions 3 that are formed to the wiring board so that the extending portions laterally extend from a position in which the semiconductor element is placed, the protruding electrodes being formed on the extending portions.

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55. The semiconductor device as claimed in claim 54, further comprising a frame 95 which supports the wiring board an which has a cavity which accommodates the semiconductor element.

56. The semiconductor device as claimed in claim 54, wherein the protruding electrodes are mechanical bumps obtained by plastic deforming the leads.

Claims 79, 82 and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of McMahon (5362656) and Kata (5897337).

At column 2, line 30 to column 4, line 27 McMahon teaches the following:

79. A semiconductor device comprising: a semiconductor device main body 14 having a semiconductor element having a surface on which protruding electrodes are directly formed, and a resin layer 44 which is formed on the surface of the semiconductor element and seals the protruding electrodes; an interposer 26 to which the semiconductor device main body is attached, a wiring pattern 30 to which the semiconductor device main body is connected being formed on a base member 28 of the interposer; an adhesive which is provided between the semiconductor device main body and the interposer and which bonds the semiconductor device main body to the interposer; a conductive member 40 which electrically connects the semiconductor device main body and the interposer; and external connection terminals 12 which are connected to the wiring pattern through holes formed in the base member and are arranged on a surface of the semiconductor device main body opposite to the surface on which the protruding electrodes are provided.

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81. The semiconductor device as claimed in claim 79, wherein the conductive member comprises stud bumps.

82. The semiconductor device as claimed in claim 79, wherein the conductive member comprises flying leads, which are integrally formed with the wiring pattern and bypasses the adhesive so as to be connected to the protruding electrodes.

83. The semiconductor device as claimed in claim 82, wherein connections of the protruding electrodes and the flying leads are sealed by resin.

However, McMahon does not appear to explicitly teach that the resin layer which is formed on the surface of the semiconductor element seals the protruding electrodes except for ends thereof. Still, as cited *supra*, Kata teaches this product. In addition, it would have been obvious to combine the product of Kata with the product of McMahon because it would facilitate device protection.

Claims 70, 72-77, 95 and 96 are allowed.

Claims 80, 84 and 85 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2<sup>nd</sup> paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

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**Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to the group receptionist at (703) 308-1782.**

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m..

The fax phone number for group 2800 is (703)305-3431.



David E. Graybill  
Primary Examiner  
Art Unit 2814

D.G.